**STM32 Families Overview**

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| Family | Core | Max Clock (MHz) | Key Features | Typical Use Cases |
| STM32F1 (e.g., STM32F103C8T6) | Cortex-M3 | 72 | Basic peripherals (USB 2.0, CAN, ADC), 20KB SRAM, 64KB Flash | Power management, ADCS backup, low-rate comms |
| STM32F4 (e.g., STM32F405RG) | Cortex-M4 (with FPU) | 168 | FPU, DSP instructions, 192KB SRAM, 1MB Flash, Ethernet, high-speed USB | Data processing, moderate DSP tasks |
| STM32F7 (e.g., STM32F767ZI) | Cortex-M7 (with FPU) | 216 | Dual-bank Flash, 512KB SRAM, Chrom-ART accelerator, Ethernet, SDRAM support | High-performance payloads, image processing |
| STM32H7 (e.g., STM32H743VI) | Cortex-M7 + M4 (dual-core) | 480 (M7), 240 (M4) | 1MB SRAM, 2MB Flash, hardware crypto, JPEG acceleration | AI/ML, real-time SDR, advanced comms |
| STM32L4 (e.g., STM32L476RG) | Cortex-M4 (with FPU) | 80 | Ultra-low-power (nA standby), 128KB SRAM, 1MB Flash, LCD interface | Power-sensitive subsystems, thermal control |
| STM32U5 (e.g., STM32U575AI) | Cortex-M33 (TrustZone) | 160 | Secure boot, PSA-certified, <1µA standby, 786KB SRAM | Secure comms, fault-tolerant systems |
| Rad-Hard Variants (e.g., STM32RH503) | Cortex-M0/M3 | 48–72 | 300 krad TID tolerance, SEL immunity, EDAC, hermetic packaging | Mission-critical OBC, long-duration missions |

**3. Performance and Technical Specifications**

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| Feature | STM32F1 | STM32F4 | STM32F7 | STM32H7 | STM32L4 | STM32U5 | Rad-Hard (STM32RH) |
| Core | M3 | M4 (FPU) | M7 (FPU) | M7+M4 (FPU) | M4 (FPU) | M33 (TrustZone) | M0/M3 |
| Max Clock (MHz) | 72 | 168 | 216 | 480 | 80 | 160 | 48–72 |
| SRAM (KB) | 20 | 192 | 512 | 1024 | 128 | 786 | 64–128 |
| Flash (KB) | 64–128 | 1024 | 2048 | 2048 | 1024 | 2048 | 256–1024 |
| FPU/DSP | No | Yes | Yes | Yes | Yes | Yes | No |
| Power (Active) | 36mA @ 72MHz | 100mA @ 168MHz | 130mA @ 216MHz | 200mA @ 480MHz | 30mA @ 80MHz | 40mA @ 160MHz | 25mA @ 48MHz |
| Standby Power | 2µA | 1µA | 1µA | 1µA | 0.3µA | 0.1µA | 0.5µA |
| Radiation Tolerance | ~50 krad (COTS) | ~50 krad (COTS) | ~50 krad (COTS) | ~50 krad (COTS) | ~50 krad (COTS) | ~50 krad (COTS) | 300 krad (qualified) |
| Key Peripherals | CAN, USB 2.0 | Ethernet, USB HS | SDRAM, LCD | Crypto, JPEG | LCD, LPUART | Secure boot | EDAC, TMR |

**4. Economic Viability**

COTS STM32s: Cost ranges from Ksh 500–3,000 (e.g., STM32F103 at ~Ksh 665, STM32H743 at about Ksh 2,600).

Rad-Hard STM32s: Ksh 50,000–500,000 (e.g., STM32RH503 at ~Ksh 300,000). COTS devices require additional mitigation (shielding, redundancy), while rad-hard variants offer reliability at a premium.

**5. Suitability for Space Applications**

**STM32F1/F4**: Best for non-critical tasks (PMU, sensor interfaces) with minimal radiation hardening.

**STM32F7/H7**: Suitable for high-performance payloads (image processing, SDR) but need external flash/SRAM hardening.

**STM32L4/U5**: Ideal for power-sensitive or secure subsystems (e.g., thermal control, encrypted comms).

**Rad-Hard STM32s**: Mandatory for long-duration missions or critical OBC functions.